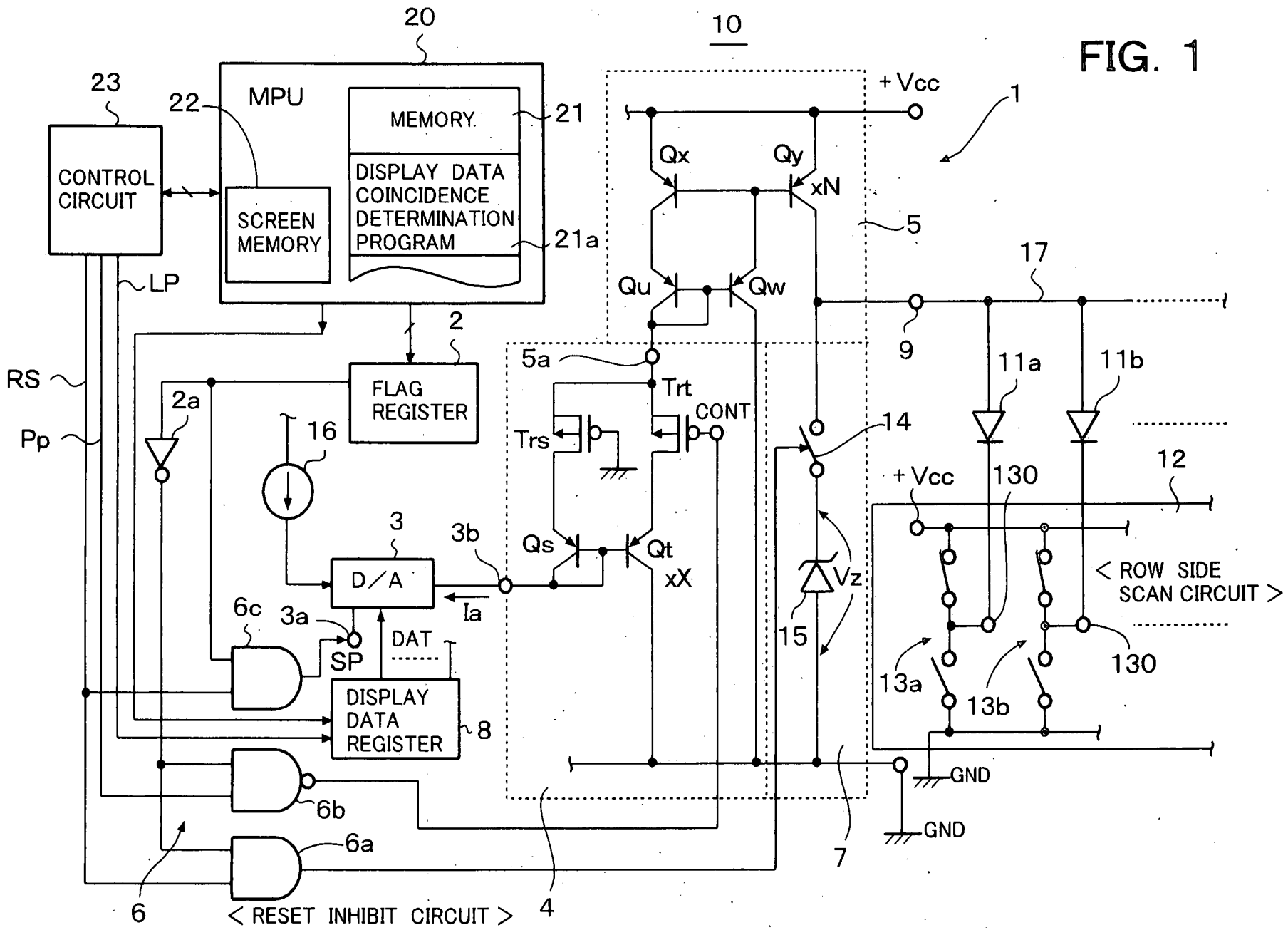

20
10
23
22
MPU
MEMORY
21
CONTROL CIRCUIT
SCREEN MEMORY
DISPLAY DATA COINCIDENCE DETERMINATION PROGRAM
21a
LP
+Vcc
1
Qx
Qy
xN
5
Qu
Qw
17
2
9
RS
FLAG REGISTER
5a
Trt
CONT
11a
11b
2a
Pp
16
Trs
14
+Vcc
130
12
3
3b
Qs
Qt
xX
D/A
Vz
< ROW SIDE SCAN CIRCUIT >
Ia
6c
3a
15
DAT
SP
130
13a
13b
DISPLAY DATA REGISTER
8
GND
6b
6a
GND
7
6
< RESET INHIBIT CIRCUIT >
4

FIG. 1

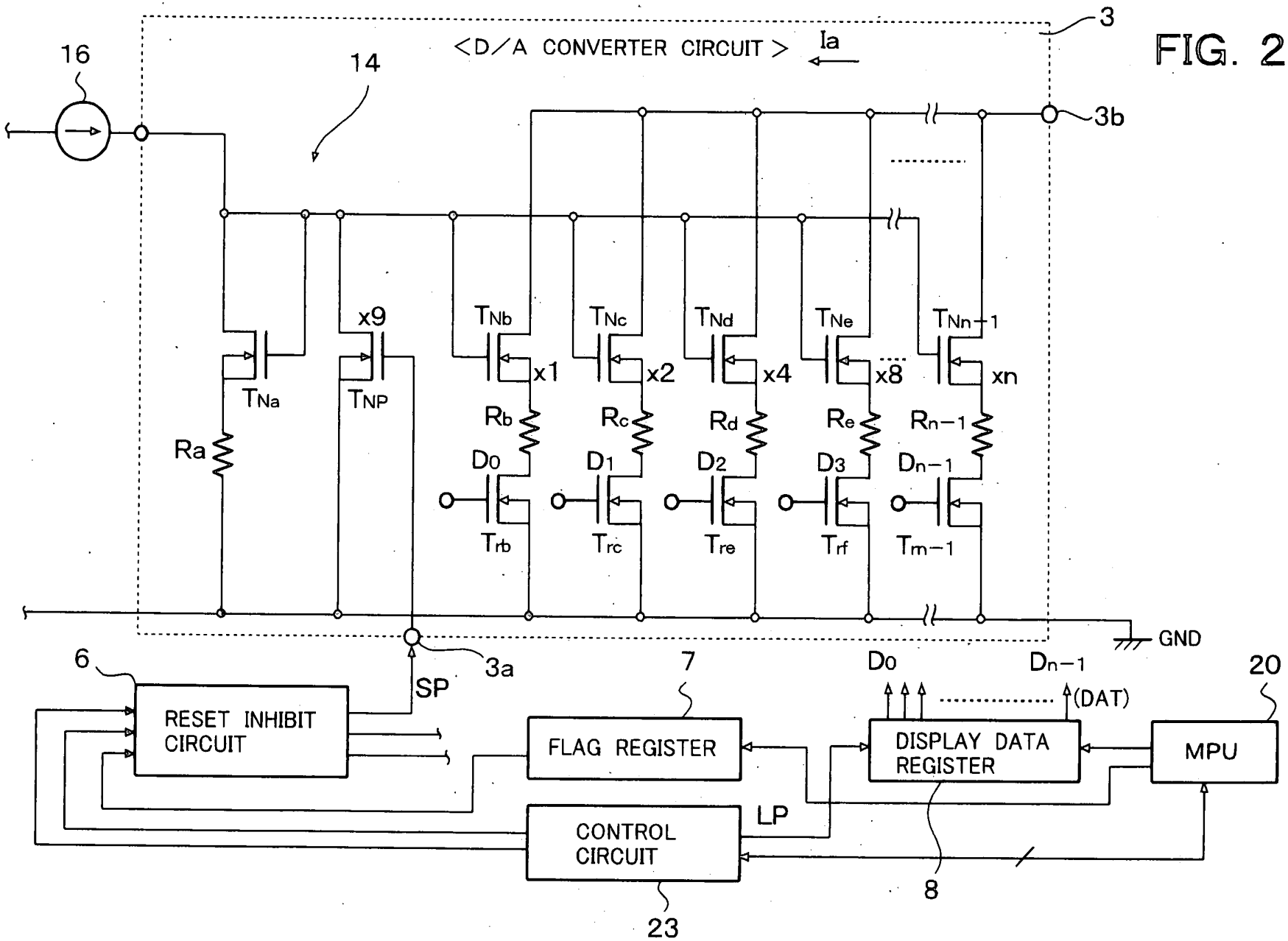

3
<D/A CONVERTER CIRCUIT>
Ia
16
14
3b
x9
TNb
TNc
TNd
TNe
TNn−1
x1
x2
x4
x8
xn
TNa
TNP
Rb
Rc
Rd
Re
Rn−1
Ra
D0
D1
D2
D3
Dn−1
Trb
Trc
Tre
Trf
Tm−1
GND
6
3a
SP
7
D0
Dn−1
20
(DAT)
RESET INHIBIT CIRCUIT
FLAG REGISTER
DISPLAY DATA REGISTER
MPU
LP
CONTROL CIRCUIT
8
23

FIG. 2

FIG. 3

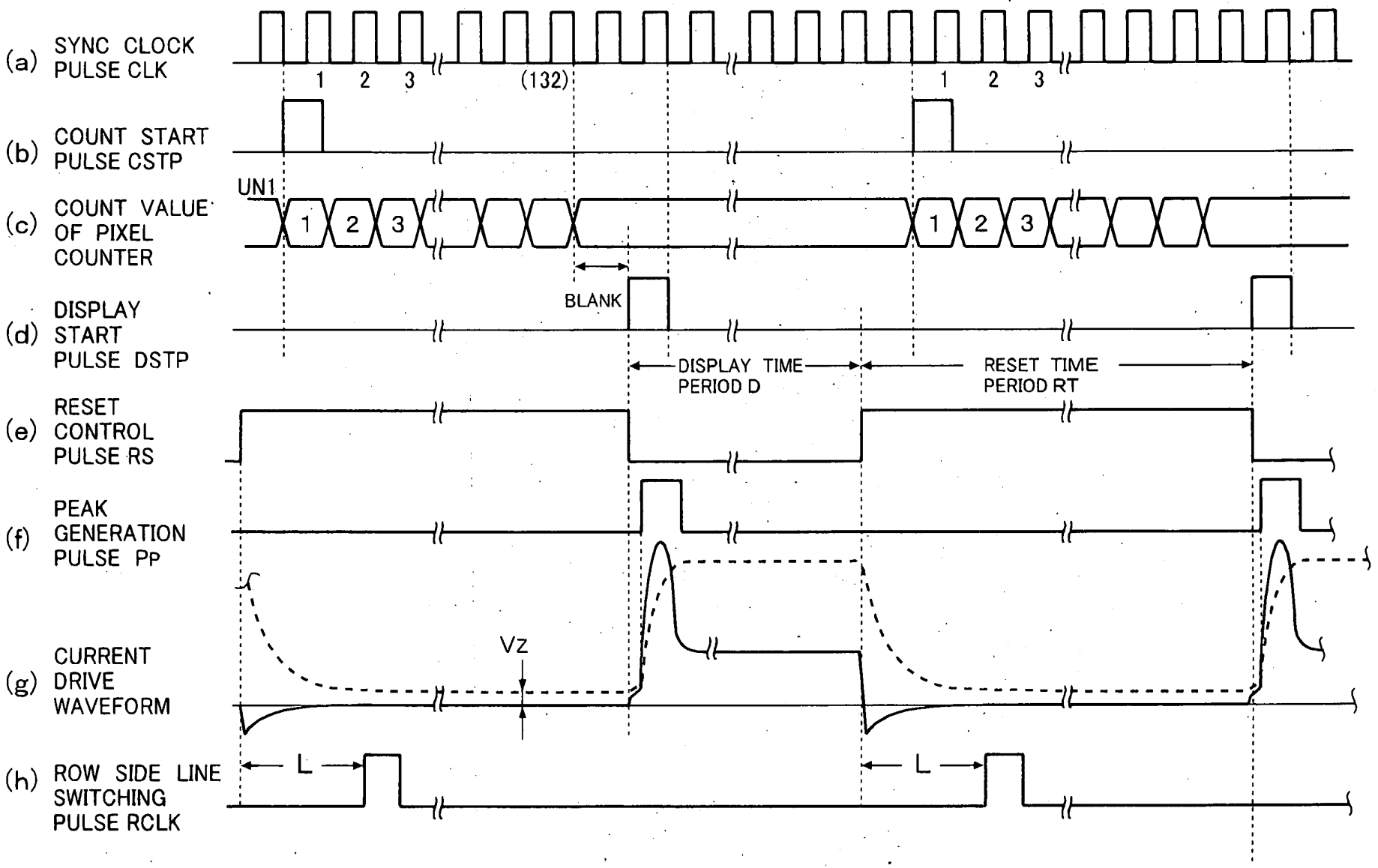

(a) SYNC CLOCK PULSE CLK
1 2 3
(132)
1 2 3
(b) COUNT START PULSE CSTP
UN1
(c) COUNT VALUE OF PIXEL COUNTER
1 2 3
1 2 3
BLANK
(d) DISPLAY START PULSE DSTP
DISPLAY TIME PERIOD D
RESET TIME PERIOD RT
(e) RESET CONTROL PULSE RS
(f) PEAK GENERATION PULSE Pp
Vz
(g) CURRENT DRIVE WAVEFORM
L
L
(h) ROW SIDE LINE SWITCHING PULSE RCLK

FIG. 4

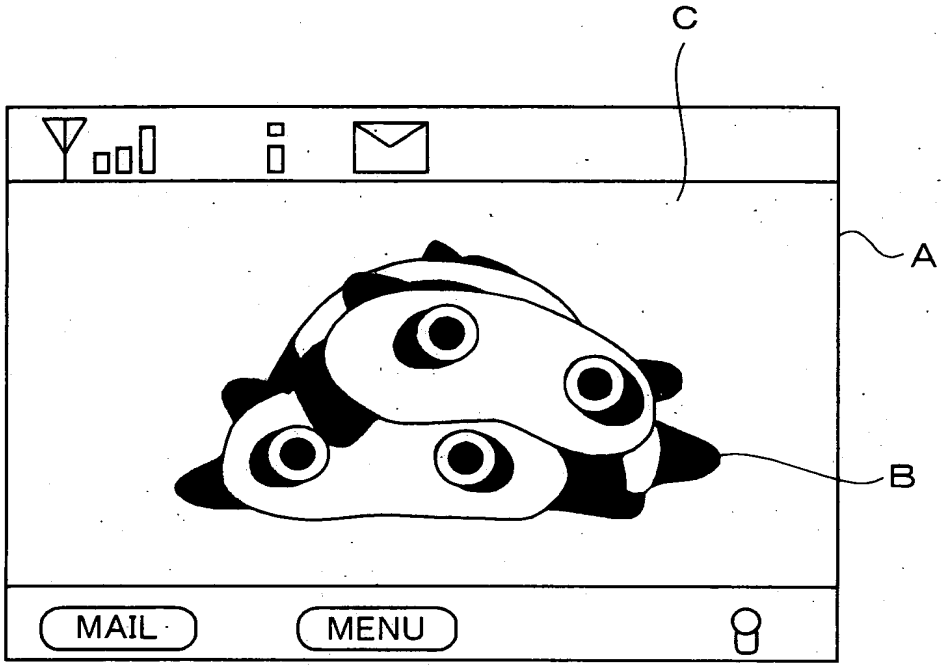
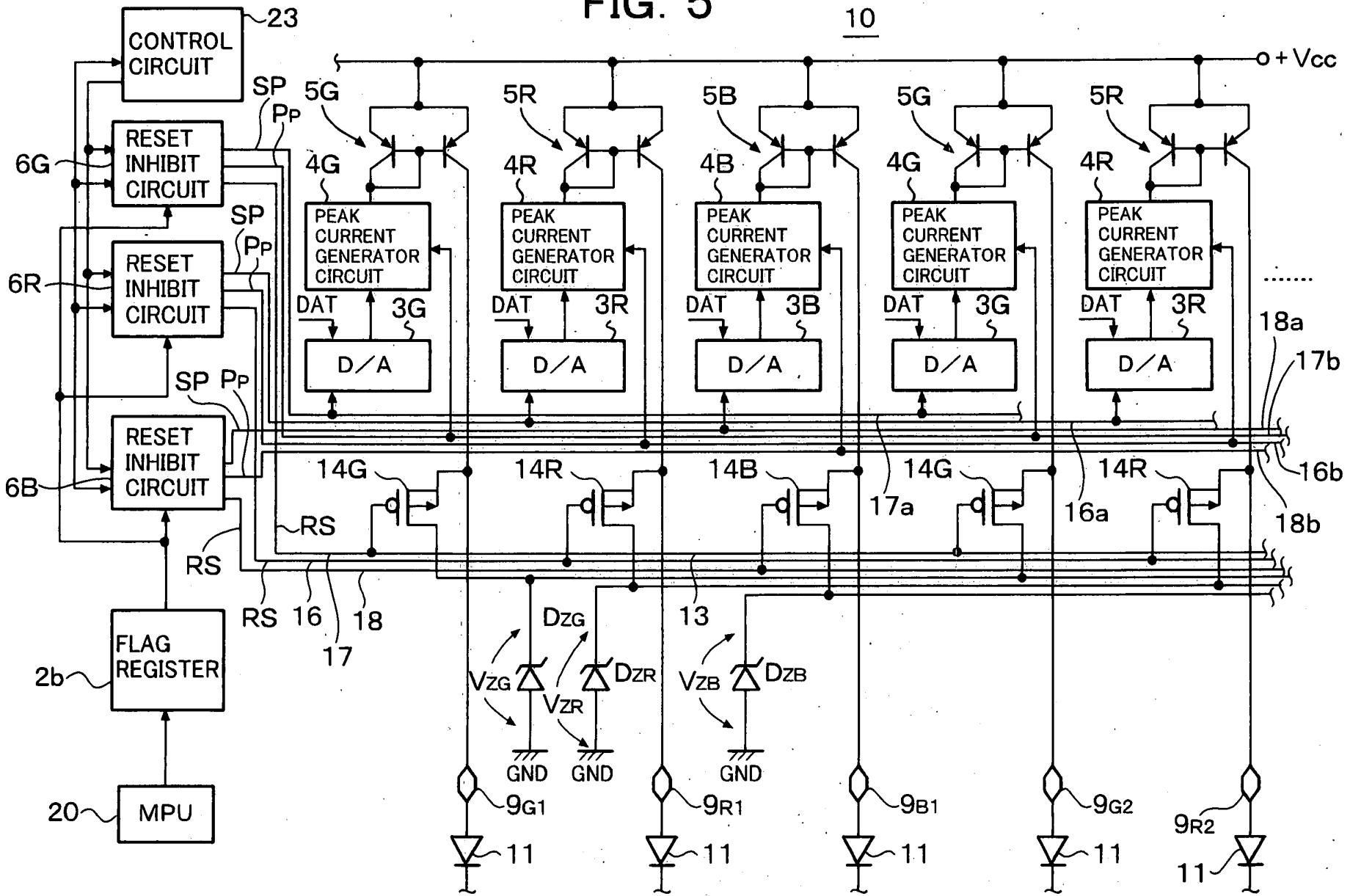


FIG. 5


10
CONTROL CIRCUIT
23
SP
PP
RESET INHIBIT CIRCUIT
6G
6R
6B
PEAK CURRENT GENERATOR CIRCUIT
DAT
3G
3R
3B
D/A
+Vcc
5G
5R
5B
4G
4R
4B
14G
14R
14B
RS
16
17
18
13
17a
16a
18a
17b
16b
18b
DZG
DZR
DZB
VZG
VZR
VZB
GND
FLAG REGISTER
2b
MPU
20
9G1
9R1
9B1
9G2
9R2
11